Amendments to the Claims

1. (original) A reference signal generator, comprising:
an oscillator that provides an oscillator signal;
a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and
a controller that adjusts said amplifier gain in response to said reference amplitude.

2. (currently amended) The generator of claim 1, wherein said amplifier gain corresponds to a gain control signal and said controller includes:
at least one comparator that responds to said reference signal and provides a pulse train when said reference amplitude exceeds a predetermined threshold signal;
in response to said pulse train, a counter that provides said gain control signal to thereby reduce said amplifier gain until said reference amplitude no longer exceeds said threshold signal
~~contoller is configured to initiate said amplifier gain at a predetermined amplifier gain and subsequently adjust said amplifier gain to a controlled amplifier gain~~.

3. (currently amended) The generator of claim 2, wherein said controller further includes:
a generator that responds to a first clock signal to provide a second clock signal, an enable signal and a subsequent disable signal;
a first gate that passes said second clock signal in response to said enable signal and blocks said second clock signal in response to said disable signal; and
a second gate that passes said second clock signal from said first gate to said counter in response to said pulse train
~~predetermined amplifier gain is a maximum amplifier gain and said controller is configured to subsequently reduce said amplifier gain to said controlled amplifier gain~~.

4. (currently amended) The generator of claim 2 [[3]], wherein said comparator is a differential pair of transistors ~~controller includes a comparator that stops reduction of said amplifer gain when said reference amplitude corresponds to a threshold amplitude.~~

5. (currently amended) The generator of claim 2, wherein said buffer amplifier includes:

at least one set of current generators that provide a current with a current amplitude that corresponds to said gain control signal; and

an inverter that carries said current to provide said reference signal with said reference amplitude thereby corresponding to said gain control signal

~~predetermined amplifier gain exceeds said controlled amplifier gain~~.

6. (currently amended) The generator of claim 5 [[2]], wherein said current generators are configured with binarily-related currents so that said current amplitude has a binary relationship to said gain control signal

~~controlled amplifier gain exceeds said predetermined amplifier gain~~.

7. (currently amended) The generator of claim 1, wherein said controller includes:

~~a clock that provides a clock signal;~~

a counter set to an initial count that maximizes said ~~ampifier~~ amplifier gain and coupled to provide a subsequent count of ~~said~~ a clock signal that reduces said ~~amplifer~~ amplifier gain; and

a comparator that terminates said subsequent count in response to said reference amplitude and a predetermined threshold amplitude.

8. (original) The generator of claim 1, wherein said buffer amplifier includes:

a plurality of resistors; and

a plurality of switches that selectively access said resistors in response to said controller to thereby adjust said amplifier gain.

9. (currently amended) The generator of claim 2 ~~1~~, wherein said at least one comparator comprises upper and lower comparators that respectively respond to

upper and lower predetermined threshold signals ~~amplifier gain is less than one~~.

10. (original) The generator of claim 1, wherein said oscillator is a digitally-controlled crystal oscillator.

11. (currently amended) A reference signal generator, comprising:
an oscillator that provides an oscillator signal;
a buffer amplifier having an ~~adjustable~~ amplifier gain that corresponds to a gain control signal and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and
a controller that adjusts said gain control signal ~~amplifier gain~~ in response to said reference amplitude.

12. (currently amended) The generator of claim 11, wherein said buffer amplifier includes a plurality of current generators ~~genrators~~ that are responsive to said gain control signal ~~controller~~.

13. (currently amended) The generator of claim 12, wherein each of said current generators includes:
a plurality of resistors; and
a plurality of switches that selectively access said resistors in response to said gain control signal ~~controller~~ to thereby adjust said amplifier gain.

14. (currently amended) The generator of claim 12 ~~11~~, wherein said buffer amplifier provides said reference signal at a reference port and each of said current generators includes:
a plurality of resistors;
a plurality of access switches that access selected ones of said resistors in response to said controller; and
an output switch that couples selected resistors to said reference port in response to said oscillator signal.

15. (currently amended) The generator of claim 16 ~~11~~, wherein said controller further includes a differential pair of amplifiers that transfers a

common mode level of said reference signal to said string of resistors ~~amplifier gain is responsive to a gain control signal and said controller includes a comparator that determines said gain control signal in response to said reference signal and a threshold signal~~.

16. (currently amended) The generator of claim 18 ~~15~~, wherein said controller further includes:

a string of resistors coupled to provide selectable voltages; and

a plurality of transistors coupled to selectively provide one of said voltages as said threshold signal.

17. (currently amended) The generator of claim 18 ~~15~~, wherein said comparator comprises a differential pair of transistors ~~that determines said gain control signal in response to said reference signal and said threshold signal~~.

18. (currently amended) The generator of claim 11, wherein ~~said amplifier gain is responsive to a digital gain control signal and~~ said controller includes:

~~a clock that provides a clock signal;~~

a counter that counts ~~said~~ a clock signal to thereby generate said digital gain control signal; and

a comparator that ~~passes~~ provides said clock signal to said counter in response to a comparison of said reference signal and a threshold signal.

19. (currently amended) The generator of claim 18, wherein said controller further includes a gate inserted to pass said clock signal to said counter in response to said comparator ~~clock includes at least one divider that divides said oscillator signal to thereby generate said clock signal~~.

20. (currently amended) The generator of claim 19 ~~11~~, wherein

~~: said buffer amplifier includes: a) a plurality of resistors; and b) a plurality of switches that selectively access said resistors in response to a gain control signal; and said controller includes a~~

said comparator generates a pulse train when said reference signal exceeds said threshold signal; and

said gate passes said clock signal in response to said pulse train

~~that provides said gain control signal in response to said reference signal and a threshold signal.~~

21. (currently amended) The generator of claim 20, wherein said controller further includes a generator that provides an enable signal to enable said gate and a subsequent disable signal to disable said gate ~~comparator comprises a differential pair of transistors that determines said gain control signal in response to said reference signal and said threshold signal~~.

22. (currently amended) The generator of claim 11 ~~18~~, wherein said controller includes:

~~a clock that provides a clock signal;~~

a counter that counts ~~said~~ a clock signal to thereby generate said gain control signal; ~~and~~

[[a]] upper and lower comparators that generate pulse trains when ~~passes said clock signal to said counter in response to a comparison of~~ said reference signal ~~and~~ exceeds [[a]] predetermined threshold signals; and

a gate that passes said clock signal to said counter in response to said pulse trains.

23. (currently amended) The generator of claim 22, wherein said controller further includes:

a differential pair of amplifiers that provides a common mode level of said reference signal; and

a string of resistors that provides said threshold signals in response to said common mode level

~~: said controller is configured to initially reset said counter to thereby provide an initial version of said gain control signal that maximizes said amplifier gain; and said counter counts said clock signal to cause said gain control signal to reduce said amplifier gain~~.

24. (currently amended) The generator of claim 22 ~~11~~, wherein said controller further includes a generator that provides an enable signal to enable

said gate and a subsequent disable signal to disable said gate ~~amplifier gain is less than one~~.

25. (original) The generator of claim 11, wherein said oscillator is a digitally-controlled crystal oscillator.

26. (currently amended) A synthesizer, comprising:
a voltage-controlled oscillator;
a phase detector that provides a control signal to said voltage-controlled oscillator;
a first frequency divider coupled between said voltage-controlled oscillator and said phase detector;
~~an~~ a reference oscillator that generates an oscillator signal;
a second frequency divider coupled between said reference oscillator and said phase detector;
a buffer amplifier having an adjustable amplifier gain and coupled to process said oscillator signal into a reference signal that has a reference amplitude; and
a controller that adjusts said amplifier gain in response to said reference amplitude.

27. (currently amended) The synthesizer of claim 29 ~~26~~, wherein said controller further includes:
a gate coupled to pass said clock signal to said counter; and
a generator that provides an enable signal to enable said gate and a subsequent disable signal to disable said gate
~~is configured to: initiate said amplifier gain at a maximum amplifier gain; and subsequently reduce said amplifier gain to a controlled amplifier gain~~.

28. (currently amended) The synthesizer of claim 29 ~~26~~, wherein said controller further includes:
a differential pair of transistors that provide a common mode level of said reference signal; and
a resistor string that provides said threshold amplitude in response to said

common mode level

~~a comparator that stops reduction of said amplifer gain when said reference amplitude corresponds to a threshold amplitude~~.

29. (currently amended) The synthesizer of claim 26, wherein said controller includes:

~~a clock that provides a clock signal;~~

a counter set to an initial count that maximizes said amplifier gain and coupled to provide a subsequent count of ~~said~~ a clock signal that reduces said amplifier gain; and

a comparator that terminates said subsequent count ~~in response to~~ when said reference amplitude reaches a threshold amplitude.

30. (original) The synthesizer of claim 26, wherein said buffer amplifier includes:

a plurality of resistors; and

a plurality of switches that selectively access said resistors in response to said controller to thereby adjust said amplifier gain.